FMTV Challenge 2016

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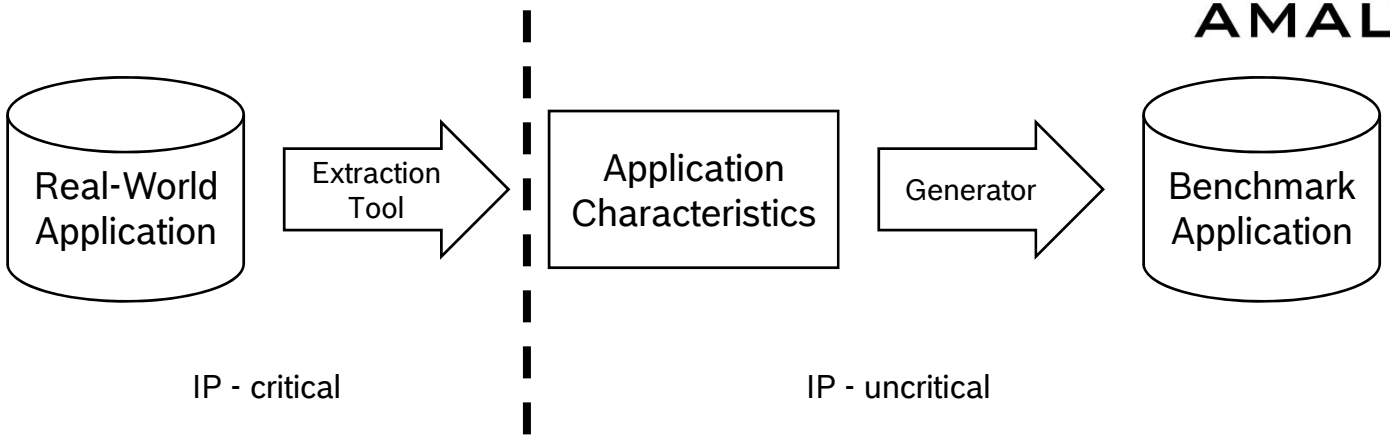
Bosch Engine Management System



- Based on the characteristics of a modern engine management system
  - S. Kramer, D. Ziegenbein, and A. Hamann, “Real world automotive benchmark for free,” in Sixth International Workshop on Analysis Tools and Methodologies for Embedded Real-time Systems (WATERS), 2015.
- Model available online:
  - http://ecrts.eit.unikl.de/forum/viewtopic.php?f=27&t=62.

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Motivation for the Challenge

- Personal observation: risk of divergence between academic research and industrial practice is currently increasing
- Analysis method need to cope with complex mechanisms of modern automotive systems to be meaningful for practical use:
  - mixed preemptive and non-preemptive priority based scheduling
  - periodic, sporadic, and engine synchronous tasks
  - multi-core platform with distributed cause-effect chains including cross-core communication
  - label (i.e. data) placement dependent execution times of runnables
- Many current approaches only address parts of the above mentioned mechanisms
- Can those approaches be extended? Can they (conservatively) approximate the behavior? How tight are the analysis results?

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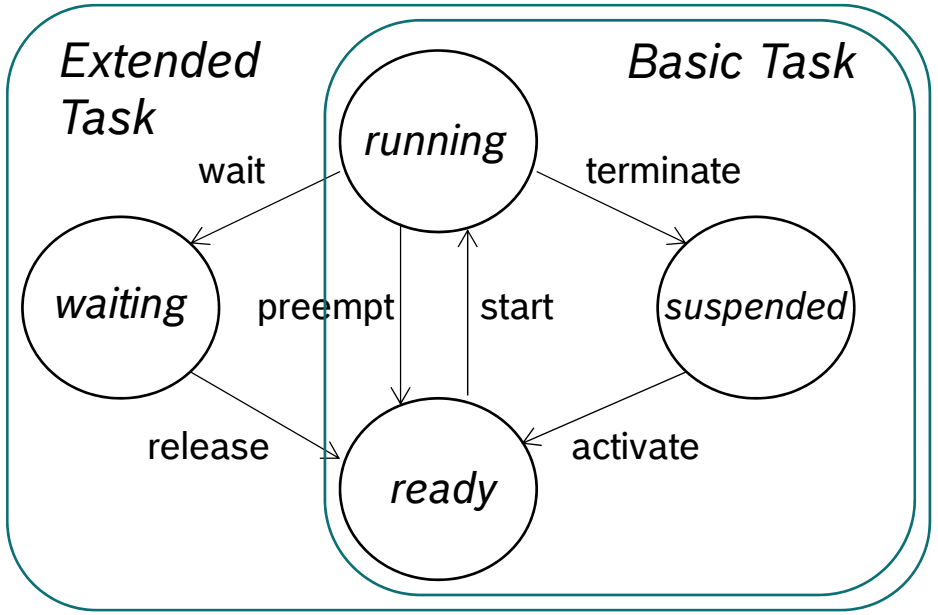
Characteristics of Automotive Software

Task

- Activation Pattern:
  - Periodic: 1 to 1000 ms
  - Angle synchronous
  - Sporadic
- Scheduled by the OS
  - Fixed Priorities
  - Preemptively or cooperatively



OSEK task states

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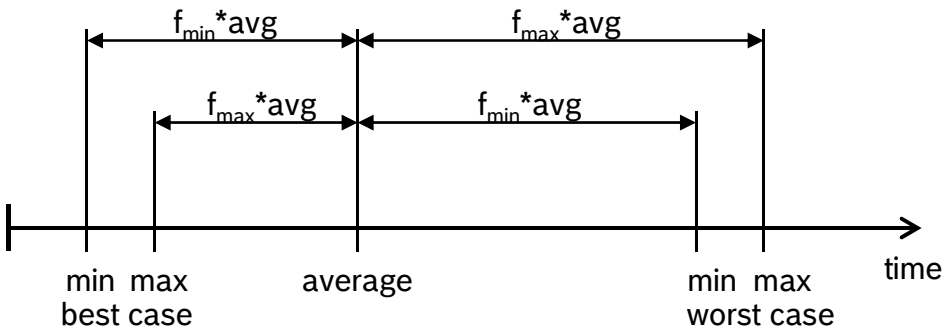
Characteristics of Automotive Software

Runnables

- Runnable are the smallest executable units
- Are grouped into tasks, according to their activation scheme

- Execution time contains:
  - code fetch
  - no label access
  - no scheduling
- assumes certain memory layout



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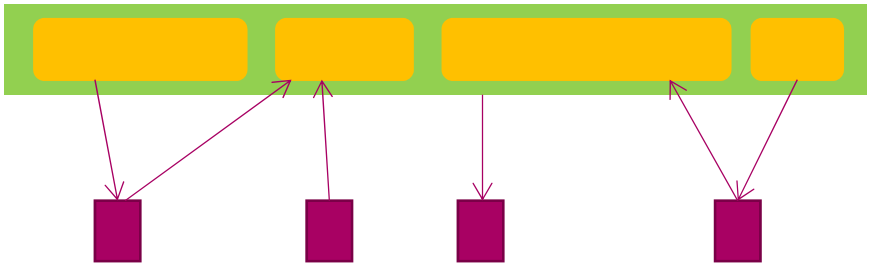
Characteristics of Automotive Software

Labels



Communication between runnables is realized with reading and writing of labels

Communication	Share
Forward	25 %
Backward	35 %
InterTask	40 %

Size	Share
Atomic (1-4 bytes)	97 %
Structs / Arrays	3 %

Access type	Share
Read-only	40 %
Write-only	10 %
Read-Write	50 %

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SW model

- Key data of the model
  - **1250 Runnables** mapped to
  - **21 Tasks & Interrupts** accessing
  - **10.000 Labels** (shared data)

- Huge amount of data dependencies
- challenge exact analysis methods

I	II	III	IV	V	VI
<10	10-50	51-100	100-500	501-1000	>1000

TABLE II. INTER-TASK COMMUNICATION

Period	1 ms	2 ms	5 ms	10 ms	20 ms	50 ms	100 ms	200 ms	1000 ms	sync
1 ms				I	I		I			I
2 ms				I	I		I			
5 ms		I	IV	IV	II	II	I			
10 ms	II	II	II	VI	IV	II	IV	II	III	IV
20 ms	I	I	I	IV	VI	II	IV	I	II	IV
50 ms			II	II	II	III	I			
100 ms		I	I	V	IV	II	VI	II	III	IV
200 ms				I	I		I	I	I	
1000 ms				III	II		III	I	IV	I
Angle-sync	I	I	I	IV	IV	I	III	I	I	V

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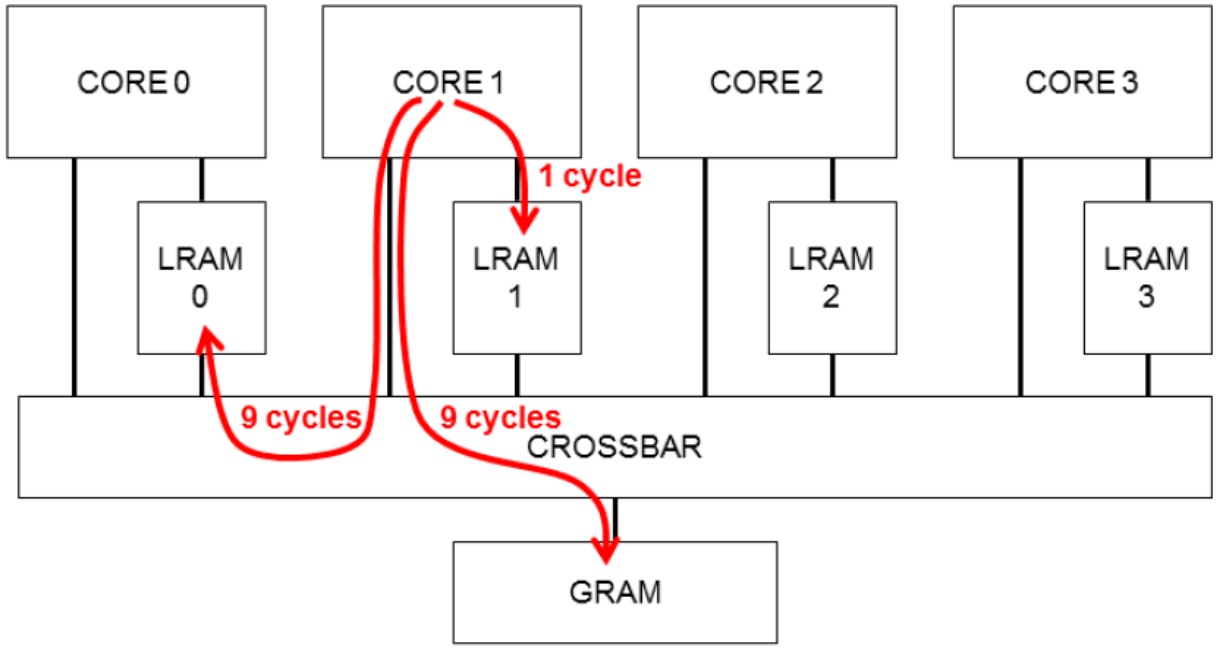
HW memory model

4public AMALTHEA
An Open Platform Project for Embedded Multicore Systems

- Access time to data in different memories (local & global)



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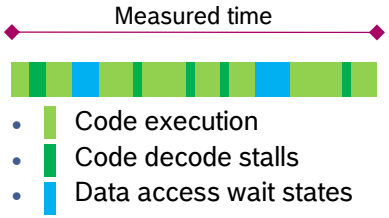
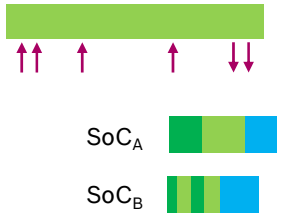
Effects of Data Access on ET

- Status Quo
  - Execution time is measured
  - Assumptions
    - Similar SW (including mapping) and identical HW
    - Labels (data) are local



- Improvements are needed for future use cases
  - More fine grained SW models to evaluate effects of code decode stalls and data access wait states
  - Effects are not negligible for upcoming platforms
    - ~ 20% of execution time is due to code decode stalls
    - ~20%-30% of execution time is due to data access wait states



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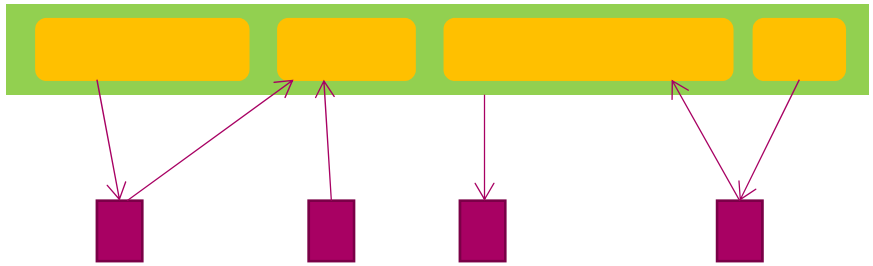
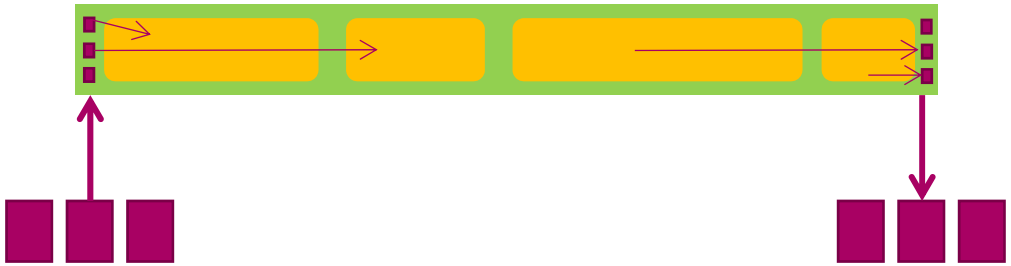
Copy Mechanism for Data Consistency

Explicit Access



Implicit Access



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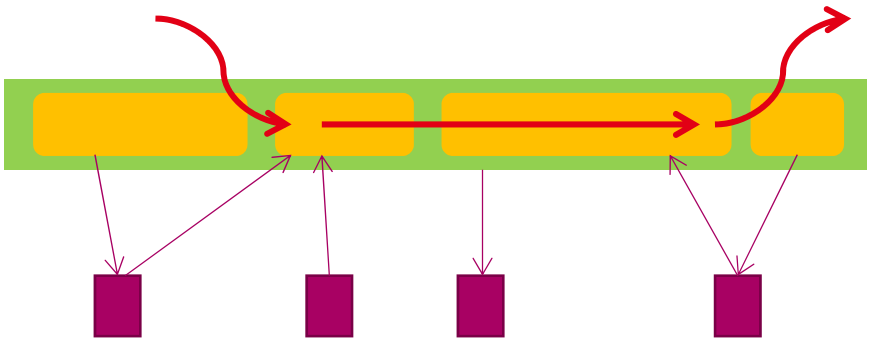
Cause-Effect Chains



Cause-Effect-Chains provide additional timing requirements that have to be met in order to ensure functional correctness

- Most chains are within one activation pattern …
- …but some span across multiple activation patterns, usually including angle synchronous domain
- Include between 2 and 5 runnables, with a write-read dependency

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Use Cases / Challenges

- Precise analysis of worst-case end-to-end latencies along complex cause-effect chains
  - mainly due to different involved periods and time domains
- Interleaved WCET and WCRT analysis
  - What is the effect on memory layout and interconnect on the execution times of runnables?
- Automatic optimized application and data mapping
- Evaluation of digital (multi-core) execution platforms
  - Which platform suits best? Especially memory layout and interconnect.
- Evaluation of software growth scenarios
  - Can the current platform accommodate anticipated future features?

Questions ?

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